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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,076	06/15/2001	Stephane G. Plante	50037.08US01	8789

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,076	PLANTE ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/17/05 amendments*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper et al (US Patent No 6,829,713 B2) in view of Fruehling et al (US Patent No 6,625,688 B1[1]).

4. As per claim 1, Cooper et al disclose a computer-implemented method for adaptively throttling a computer, comprising:

measuring a prior utilization of the computer [Fig. 4-6; col. 8; line 16, 51; determining a utilization of a central processing unit]; and

if the prior utilization crosses a threshold, modifying a parameter associated with the CPU [Fig. 4-6; col. 5, line 35 -- col. 6, line 3; col. 8, lines 16-33].

Cooper et al do not expressly disclose about determining the utilization of the CPU while the CPU is idle. But, Cooper et al disclose that the utilization request may be periodic or may occur in response to relevant power management events such as thermal or processor workload events [col. 5, lines 38-42; emphasis added]. However, Fruehling et al expressly disclose about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no workload) to determine the CPU utilization. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

5. As per claim 11, Cooper et al disclose a computer-readable medium having computer executable instructions for adaptively throttling a computer including a CPU having a CPU performance level [Fig. 1a, 1b, 4-6], comprising:

calculating a prior utilization of the CPU [Fig. 4-6; col. 8; line 16, 51; determining a utilization of a central processing unit]; and

calculating a utilizable CPU performance level using the prior utilization [Fig. 4-6; col. 5, line 35 -- col. 6, line 3; col. 8, lines 16-33].

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[1] Prior art cited by examiner in the prior office action (dated 11/15/04).

Cooper et al do not expressly disclose about determining the utilization of the CPU while the CPU is idle. But, Cooper et al disclose that the utilization request may be periodic or may occur in response to relevant power management events such as thermal or processor workload events [col. 5, lines 38-42; emphasis added]. However, Fruehling et al expressly disclose about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no workload) to determine the CPU utilization. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

6. As per claim 18, Cooper et al disclose a system for adaptively throttling a computer including a CPU having a CPU performance level [Fig. 1a, 1b, 4-6], comprising:

a CPU utilization monitor configured to monitor a utilization of the CPU [Fig. 4-6; col. 8; line 16, 51; determining a utilization of a central processing unit; col. 5, line 35 -- col. 42];

a CPU throttler configured to perform the adaptive throttling of the CPU based on information from the CPU utilization monitor [Fig. 4-6; col. 5, line 35 -- col. 6, line 3; col. 8, lines 16-33; throttling the CPU]; and

a timer configured to monitor a time since an idle state [col. 1, lines 62-66; idle for a predetermined period of time; col. 5, lines 38-42; processor workload events; col. 6, lines 15-21; duration of time that the CPU remains at a particular state].

Cooper et al do not expressly disclose about activating the CPU throttler when the CPU enters an idle state. But, Cooper et al disclose that the utilization request may be periodic or may occur in response to relevant power management events such as thermal or processor workload events [col. 5, lines 38-42; emphasis added]. However, Fruehling et al expressly disclose about a CPU performing a comparison task during an idle cycle of the CPU [Fig. 6B, 6D, 7A; detect CPU_idle_Bus; col. 18, lines 4-7, 43, 50; col. 20, lines 1-8; col. 11, lines 32-34; col. 12, lines 60-63; col. 13, lines 46-47]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CPU idle cycle (i.e., while there is no workload) to determine the CPU utilization and activate the CPU throttler. Moreover, it would clearly be a time efficient to utilize the idle cycle of the CPU to determine the utilization of the CPU and throttle it accordingly.

7. As per claim 2, Cooper et al disclose that the parameter comprises a clock frequency [col. 1, lines 39-45; col. 6, lines 10-12; clock frequency].

8. As per claim 3, Cooper et al disclose that the parameter comprises a voltage [col. 1, lines 27-40, 62-66].

9. As per claim 4, Cooper et al disclose storing the prior utilization in a utilization history database [col. 5, line 35 -- col. 6, line 3; comparing with threshold value stored in the system; col. 6, lines 22-31; user-defined power management profile].

10. As per claim 5, Cooper et al disclose accessing the utilization history database to determine if the CPU has been at a performance level for a sufficient period of time [col. 1, lines 62-66; idle for a predetermined period of time; col. 6, lines 15-21; duration of time that the CPU remains at a particular state; col. 6, lines 22-31; user-defined power management profile].

11. As per claim 6, Cooper et al disclose that the threshold indicates that a performance level allocated with the CPU should be increased [col. 5, line 35 -- col. 6, line 3].

12. As per claim 7, Cooper et al disclose applying a system policy to determine whether to increase the performance level of the CPU [col. 6, lines 22-58; user-defined power management profile].

13. As per claim 8, Cooper et al disclose that the system policy comprises a heat performance limit related to a temperature sensed near the CPU [col. 5, lines 35-42; thermal; col. 6, lines 22-58; user-defined power management profile].

14. As per claim 9, Cooper et al disclose that the system policy comprises a battery performance limit related to a battery level of a battery supplying the computer with power [col. 6, lines 22-58; user-defined power management profile is checked to ensure maximum battery mode].

15. As per claim 10, Cooper et al disclose that the system policy relates to a switching latency of the CPU [col. 22-25; latency associated with re-activation; col. 6, lines 22-58; user-defined power management profile].

16. As per claim 12, Cooper et al disclose calculating a thermal CPU performance limit [col. 5, lines 35-42; CPU utilization status in response to relevant power management event such as thermal]; and changing the CPU performance level [col. 5, line 35 -- col. 6, line 3].

17. As per claim 13, Cooper et al disclose calculating a battery CPU performance limit [col. 6, lines 22-58; the system optimizes the battery life]; and changing the CPU performance level [col. 6, lines 22-58].

18. As per claim 14, Cooper et al disclose changing the CPU performance level to utilizable CPU performance level [col. 5, line 22 -- col. 6, line 58].

19. As per claim 15, Cooper et al disclose changing the CPU performance level occurs at an expiration of a timer [col. 1, lines 62-66; idle for a predetermined period of time; col. 5, lines 38-42; processor workload events; col. 6, lines 15-21; duration of time that the CPU remains at a particular state; col. 5, line 35 -- col. 6, line 3].

20. As per claim 16, Cooper et al disclose if the minimum performance is equal to a maximum performance level of the CPU, disabling the timer [inherent to the system as there is no more performance level for change].

21. As per claim 17, Cooper et al disclose if the new performance level is less than a maximum performance level of the CPU, resetting the timer [inherent to system as there is more than one performance level for change].

22. As per claim 19, Cooper et al disclose that the CPU is activated when the time since the last idle state exceeds a threshold [col. 1, lines 62-66; idle for a predetermined period of time; col. 5, lines 38-42; processor workload events; col. 6, lines 15-21; duration of time that the CPU remains at a particular state; col. 5, line 35 -- col. 6, line 3].

23. As per claim 20, Cooper et al disclose that a thermal policy manager configured to monitor a temperature near the CPU wherein the thermal policy manager activates the CPU throttler when the temperature crosses a threshold [col. 5, lines 35-42; thermal; col. 6, lines 22-58; user-defined power management profile].

24. As per claim 21, Cooper et al disclose a degradation policy manager configured to receive a charge level from a battery sensor monitoring a battery wherein the degradation policy manager activates the CPU throttler when the charge level crosses a threshold [col. 6, lines 22-58].

25. As per claim 22, Cooper et al disclose that the CPU throttler changes the CPU performance level in response to a utilization of the CPU measured by the CPU utilization monitor [Fig. 4-6; col. 8; line 16, 51; determining a utilization of a central processing unit; col. 5, line 35 -- col. 6, line 3; col. 8, lines 16-33; throttling the CPU].

26. As per claim 23, Cooper et al disclose that upon activation, the CPU throttler resets the timer [col. 1, lines 62-66; idle for a predetermined period of time; col. 6, lines 15-21; duration of time that the CPU remains at a particular state; inherent to the system].

Response to Arguments

27. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
April 13, 2005